IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Paul Scott et al.		
Assignee:	Cypress Semiconductor Corporation		
Title:	METHOD, ARCHITECTURE AND CIRCUITRY FOR CONTROLLING PULSE WIDTH IN A PHASE AND/OR FREQUENCY DETECTOR		
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Commissioner for Patents
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DECLARATION OF PAUL SCOTT PURSUANT TO 37 C.F.R. § 1.132

I, Paul Scott, hereby declare as follows:

1. I am presently employed as Vice President of Product Planning by Cypress Semiconductor Corporation.

2. I have been employed by Cypress since 1991 in various capacities.

3. I have reviewed the claims of the present invention and the background of the present invention.

4. I understand that in one embodiment the present invention concerns:

An apparatus comprising:

a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a first multi-phased clock signal and (ii) two or more serial data signals; and

a second circuit configured to present said two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

5. I understand that in another embodiment the present invention concerns:

A circuit comprising:

means for generating a parallel output data signal in response to (i) a selected phase a plurality of phases of a multi-phased first clock signal and (ii) two or more serial data signals; and

means for generating said two or more serial data signals and said multi-phased first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

6. I understand that in another embodiment the present invention concerns:

A method for controlling a pulse width in a phase and/or frequency detector comprising the steps of:

(A) generating a parallel output data signal in response to (i) a selected phase of a plurality of phases of a multi-phased first clock signal and (ii) two or more serial data signals; and

(B) generating said two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal, wherein said multi-phased first clock signal is configured to control said pulse width.

7. The assertion on page 2, third paragraph, in the Office Action that any clock signal has "some" phase is not completely correct.

8. Phase is typically a measurement of a signal relative to some baseline. A signal does not have a phase with respect to itself.

9. The assertion that "the phase of the clock signal will be selected by the RXPLL (22) before outputting the clock signal" is not supported by the background section. Box 22 of the background is a PLL that adjusts frequency to track incoming data.

10. The background section is silent regarding a phases of a clock signal.

11. The background is also silent regarding a multi-phased clock signal. The background section does not show a plurality of phases of a clock signal.

12. It follows that the background is silent regarding a selected phase of a plurality of phases of a first multi-phased clock signal, as presently claimed.

13. The Office Action makes the assertion that "a new different phase will be selected by the PLL according to certain criteria, such as adjustments done in the PLL." Adjustments in a PLL are typically made to the frequency to manage phase.

14. The background section, on its face, does not disclose or suggest a selected phase, as presently claimed.

15. I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or patents issued therefrom.

Paul H Scott Date: 1/28/2005

Paul Scott